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Insights into the Interfacial Properties of Low-Voltage CuPc Field-Effect Transistor

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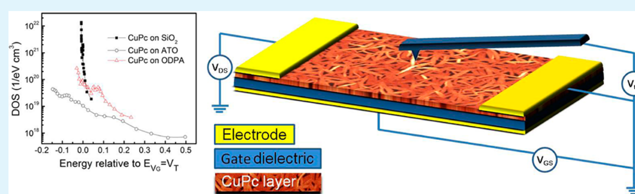
Supporting Information

ABSTRACT: The interfacial transport properties and density of states (DOS) of CuPc near the dielectric surface in an operating organic field-effect transistor (OFET) are investigated using Kelvin probe force microscopy. We find that the carrier mobility of CuPc on high-k Al_2O_y/TiO_x (ATO) dielectrics under a channel electrical field of 4.3×10^2 V/cm reaches 20 times as large as that of CuPc on SiO_2. The DOS of the highest occupied molecular orbital (HOMO) of CuPc on the ATO substrate has a Gaussian width of 0.33 ± 0.02 eV, and the traps DOS in the gap of CuPc on the ATO substrate is as small as 7×10^{17} cm^{-3}. A gap state near the HOMO edge is observed and assigned to the doping level of oxygen. The measured HOMO DOS of CuPc on SiO_2 decreases abruptly near $E_{V_{GS} = V_T}$, and the pinning of DOS is observed, suggesting a higher trap DOS of 10^{19}–10^{20} cm^{-3} at the interface. The relationships between DOS and the structural, chemical, as well as electrical properties at the interface are discussed. The superior performance of CuPc/ATO OFET is attributed to the low trap DOS and doping effect.



KEYWORDS: *organic field-effect transistor, density of state, Kelvin probe force microscopy, interface, high-k*

INTRODUCTION

Organic field-effect transistors (OFETs) have been one of the most attractive research areas in recent years because of their low cost, low processing temperature, and potential applications in flexible displays,[1] electronic papers,[2] and sensors.[3] Although impressive progress in the electrical performance has been made over the past decade,[4−7] major limitations that hamper the applications of OFETs are the low carrier mobility and high operating voltage in organic semiconductors. One feasible solution to these critical issues is to use high-k insulators as gate dielectrics, which allows one to attain high induced charge carrier density in the conducing channel at a low gate voltage. A few low-voltage OFETs utilizing organic and inorganic high-k materials as gate dielectrics have been demonstrated in recent years.[8,9] Polymers are one group of attractive high-k dielectrics for their solution-processed and low-temperature fabrication. However, the limitation of polymer insulators is that the thickness is normally larger than 100 nm, and therefore an operation voltage lower than 3 V is not easy to achieve.[8] The thickness of inorganic dielectrics, such as Al_2O_3, HfO_2, and Ta_2O_5, can be decreased to tens of nanometers or even smaller, and the k value can be very high. Unfortunately, they still suffered from poor crystalline structure or high interfacial traps.[10] More importantly, it is observed that the mobility decreases with increasing k value, which suggests a contradiction between low-voltage operation and high device mobility.[11−13] The density of states (DOS) broadening due to high dipolar disorder at the interface of high-k dielectrics is proposed to interpret the k-dependent mobility by Veres et al.;[13] on the other hand, Hulea et al. attribute the above phenomenon to the formation of Fröhlich polarons at the interface.[11] Although the mechanism is still not clear, it indicates that an understanding of the interfacial DOS of organic/high-k dielectrics is a critical issue for further improvement of the OFET performance.

DOS is one of the most important properties that determines carrier transport in OFETs.[5] Accurate knowledge of the DOS in organic semiconductors can be revealed by photoelectron emission spectroscopy.[14,15] Novel methods, such as the space-charge-limited-current (SCLC) method[16] and Kelvin probe force microscopy (KPFM) method,[17,18] have been proposed in the recent years, by taking advantage of in situ measurement of bulk and interfacial DOS in a working device. In organic semiconductors, van der Waals-type intermolecular interaction is very different from the covalent bonding of inorganic semiconductors;[19] however, the shape of the DOS in single-crystal pentacene is found to resemble that of hydrogenated amorphous silicon.[20] A comparison between the DOS of

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several organic thin-film and single-crystal field-effect transistors (FETs) measured by the SCLC method was recently reviewed by Kalb et al.[19] Nevertheless, the understanding of the DOS at the interface of working OFETs, especially the influences of doping, defects, and the substrate, are still preliminary. Meanwhile, challenges exist in the utilization of high-*k* dielectrics to reduce the high driving voltage of OFETs,[21] and a quantitative investigation of the effect of high-*k* gate dielectrics on the DOS is lacking.

In our recent experiment, we have fabricated low-voltage CuPc FETs using a high-*k* Al_2O_y/TiO_x (ATO) thin film as a gate dielectric, which possesses an equivalent *k* value of about 13.3.[21] The mobility of the FETs has exceeded 0.1 $cm^2/V{\cdot}s$, which is better than most of the CuPc FETs. In the present study, we will systematically investigate the nanostructural and electrical properties at the CuPc/dielectric interface using the KPFM method. KPFM has been widely used in organic devices to determine the interfacial energy level alignment,[22] device potential distribution,[23] contact effect,[24,25] and so on. Besides, Tal et al. show that KPFM can be used to investigate the real DOS at the interface of an operating OFET with high spatial resolution.[17] By using KPFM, we measure the DOS at the interface of CuPc/dielectric and then discuss its relationship with the crystalline structure, doping, and chemical status of the dielectric surface.

■ EXPERIMENTAL SECTION

A thermally oxidized 300-nm-thick SiO_2 on an n^{++}-Si wafer and a 45-nm-thick ATO on an n^{++}-Si wafer are used as substrates for the fabrication of CuPc FETs (the detailed experimental procedure is given in the Supporting Information). CuPc films with a thickness of 30 nm are deposited onto the substrates under a pressure of about 3×10^{-4} Pa and a deposition rate of about 0.1 Å/s with a substrate temperature of 180 °C. The 30-nm-thick gold was subsequently deposited onto the organic layer as source and drain electrodes through a shadow mask with a deposition rate of about 0.3 Å/s. In the DOS and in situ surface potential measurement using KPFM in air conditions, the channel region must be fully covered by the CuPc thin film; at the same time, the thin film thickness should be maintained thin enough to minimize the band-bending effect in the organic layer. Therefore, devices with 5-nm-thick CuPc thin films are used in these measurements.

The electrical characteristics of the OFETs are measured in air using a Keithley 4200 SCS. The morphologies and DOS measurements are characterized by DI D3100 atomic force microscopy (AFM) in air. A schematic measurement of the device potential using KPFM is shown in Figure S1 in the Supporting Information. In the DOS measurement, the surface potential is taken after a 2 min delay at each voltage step. Therefore, the measured DOS can be regarded as the steady-state DOS. Because the measurements take a long time, thermal drift can be observed in the experiment. However, the surface potential is uniform on the CuPc surface, especially in the CuPc/ATO case, so the thermal drift effect does not affect our analysis. Moreover, in order to reduce the noise level and the effect of thermal drift, we calculate the DOS by average over 10 curves from 10 positions in the center of the channel. A detailed description of the DOS measurement by KPFM can be found in ref 18. The two-dimensional grazing-incidence X-ray diffraction (GIXD) patterns were obtained at beamline BL14B1 (λ = 1.24 Å) of the Shanghai Synchrotron Radiation Facility with an incident angle of 0.06°. A goniometer from Solon Tech. Co. Ltd. (Shanghai) is adopted to test the contact angle of the substrates.

■ RESULTS AND DISCUSSION

The 30-nm-thick CuPc/ATO OFET shows a high mobility larger than 0.1 $cm^2/V{\cdot}s$, while the mobility of the 30-nm-thick $CuPc/SiO_2$ OFET is on the order of 10^{-3} $cm^2/V{\cdot}s$. During the operation of OFETs, the first several layers near the interface are the locus of charge carrier transport. To reveal the interfacial charge-transport behavior, we applied KPFM measurement on the working device with a 5-nm-thick CuPc channel to characterize the DOS at the interface. Figure 1

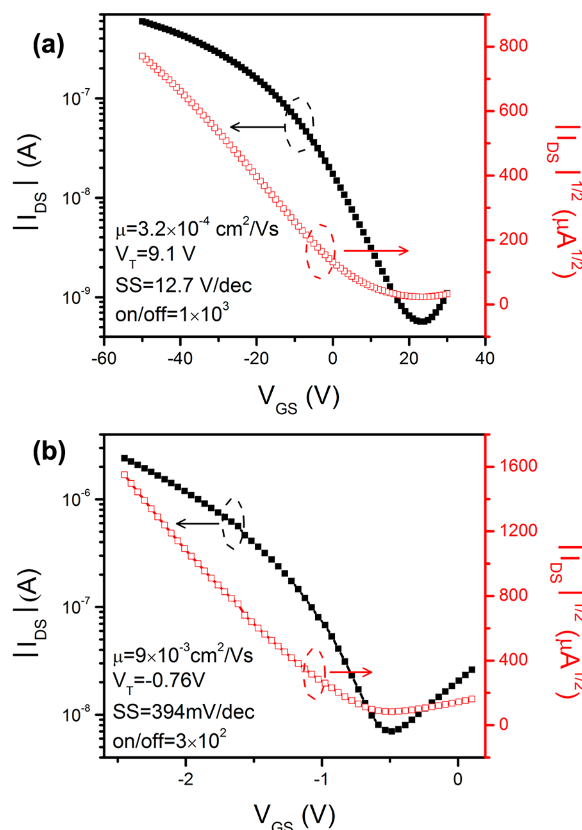

Figure 1. Transfer curves of 5-nm-thick CuPc OFETs with SiO_2 (a) and ATO (b) gate dielectrics, respectively.

shows that the 5-nm-thick CuPc device with a SiO_2 dielectric works at a high V_{GS} of −50 V and the mobility is 3.2×10^{-4} $cm^2/V{\cdot}s$. Notably, the CuPc device on ATO operates at low V_{GS} of −2 V and exhibits a higher mobility of 9.0×10^{-3} $cm^2/V{\cdot}s$. Although reducing the thickness of organic layer will lead to a decrease of mobility,[26,27] the 5-nm-thick devices exhibit *I*−*V* characteristics similar to those of their thicker devices, which ensure that the following measurement can derive the real interfacial properties in working condition.

The surface potential profiles along the devices are shown in Figure S2 in the Supporting Information. The resistance at the contacts and the channel can be calculated separately from the surface potential profile, and the results are shown in Figure 2a,c. Both plots show that the resistance decreases rapidly as V_{DS} is applied, indicating that the device required a small transverse electrical field to activate the carrier hopping along the channel and injection from the contacts. The channel and drain contact resistances reach the minimum values because of the pinch-off at the drain electrode. We find that the minimum resistance of the CuPc channel on ATO is 3.1 MΩ. This value is about one-tenth of that in the $CuPc/SiO_2$ device (34.0 MΩ). Further increasing V_{DS} leads to depletion near the drain electrode; therefore, a dramatic increase of resistance of the channel and drain contact at higher V_{DS} is observed.

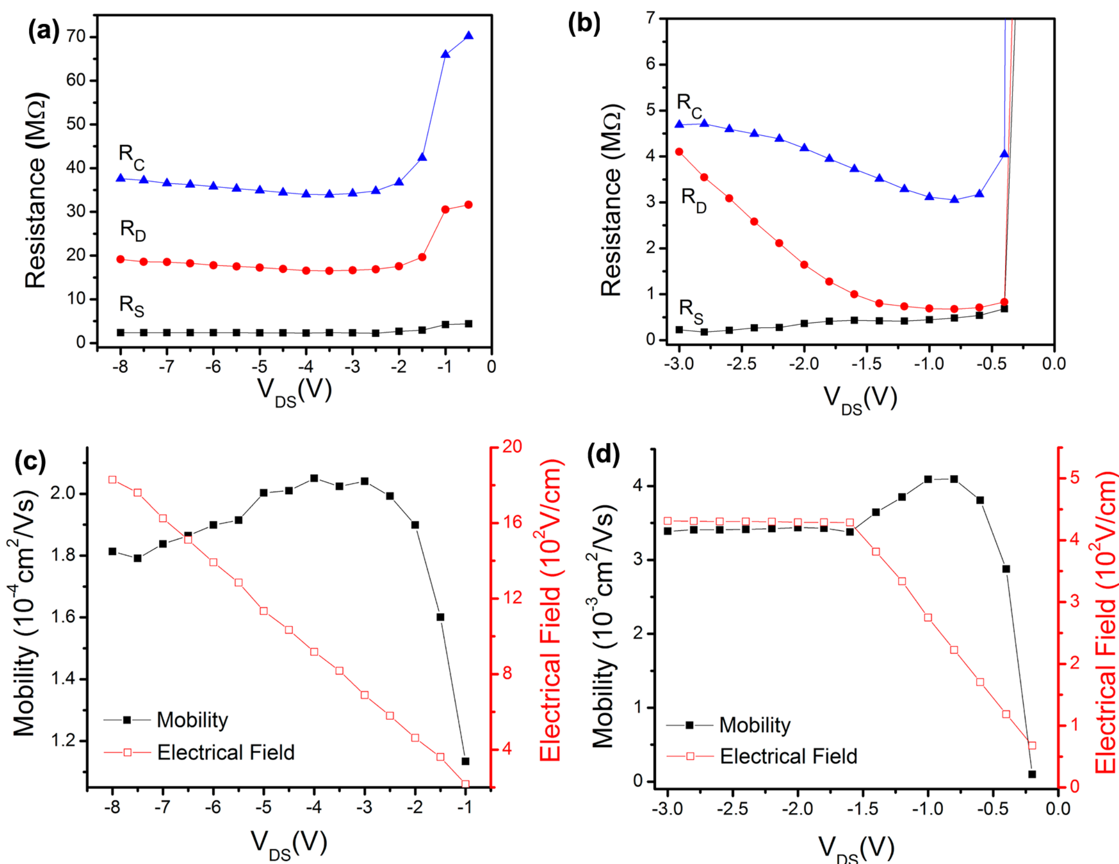

Figure 2. (a and b) Source, drain, and channel resistances of CuPc/SiO_2 and CuPc/ATO devices, respectively. (c and d) V_{DS}-dependent mobility and channel electrical field of CuPc/SiO_2 and CuPc/ATO devices, respectively.

By using the potential profiles, we are able to calculate the intrinsic mobility of the channel regions in CuPc thin-film transistors (TFTs). The channel regions with linear surface potential drops are (Figure S2 in the Supporting Information) considered using the following equation:

$$I_{DS} = eWn(x)\ \mu(V_g', E)\ E(x) \tag{1}$$

where W is the channel length and e is the elemental charge. $E(x)$ is the local electrical field that can be determined by $-\partial V$ ∂x from the measured surface potential profile. The interfacial carrier density $n(x)$ is given by $C_{ox}(V_{GS} - V_t)/e$. The applied V_{DS} will change the carrier density in the channel, which may cause errors in calculation. This is why we observed a drop of mobility at high V_{DS}. At low V_{DS}, its effect on the carrier density near the source electrode is very small. Practically, we observe that the electrical field increases linearly with increasing V_{DS} between −1 and −8 V for SiO_2 and between −0.2 and −1.4 V for ATO, suggesting that the carrier density near the source electrode is not obviously affected by V_{DS}. At the same time, the highest electrical field near the source electrode in the CuPc/ATO device is only 4.3×10^2 V/cm, which is much smaller than that in the CuPc/SiO_2 device; however, the maximum mobility derived is 4.09×10^{-3} $cm^2/V{\cdot}s$ for the CuPc/ATO device. This value is about 20 times larger than that of the CuPc/SiO_2 device (2.04×10^{-4} $cm^2/V{\cdot}s$).

Figure 3 shows the DOS of CuPc on different dielectrics. CuPc is a p-type organic semiconductor in ambient conditions; thus, the DOS measured by the KPFM method represents the highest occupied molecular orbital (HOMO) structure. The measured DOS of CuPc on SiO_2 exhibits a drastic decrease of DOS near $E = 0$ eV. A similar phenomenon is also observed by Celebi et al. at the interface of CuPc/OTS/SiO_2 in ultrahigh-

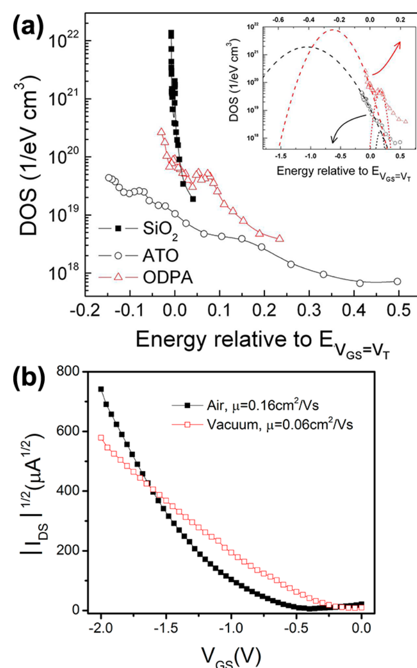

Figure 3. (a) DOS of 5-nm-thick CuPc thin films on SiO_2, ATO, and ODPA/ATO substrates. The inset shows the fitting of the DOS using Gaussian distribution. (b) Transfer curves of a 30-nm-thick CuPc/ATO OFET device in air and in vacuum of 10^{-5} Pa.

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vacuum conditions.[28] In addition, they observe an exponential decrease of the DOS with an characteristic energy of 0.11 eV. Interestingly, the measured surface potential changes immediately after alteration of the gate bias and then recovers slowly (Figure S1c in the Supporting Information) in our case. The stable surface potential is pinned at about 80 meV below the surface potential of the gold electrode.

Under ambient conditions, H_2O, hydroxyl groups, and O_2 are the key factors that can greatly affect the performance of OFETs. The presence of H_2O and hydroxyl groups on the dielectric surface is always detrimental to charge transfer. On the SiO_2 surface, the interfacial Si−O−H dangling bond is not only an electron trap but also a trap for holes. Trap formation due to water diffusion and absorption on a SiO_2 substrate by gate bias stress has been observed.[29] Therefore, the pinning of the DOS on SiO_2 is due to the formation of traps under ambient conditions. It has been reported that, after OTS modification, bias-dependent trap formation is not observed,[29] which can explain the observed DOS tail reported by Celebi et al.[28] Our results reveal that the concentration of traps is around the order of 10^{19}−10^{20} cm^{-3} at the interface between CuPc and SiO_2. The effect of oxygen is not observed at the CuPc/SiO_2 interface because its density is far below that of the trap states (see below).

On the other hand, the observed DOS distribution at the interface of CuPc on ATO is wider, but the concentration is much lower than that of CuPc/SiO_2. In addition, several small broad peaks can be observed in the DOS, which suggests that the CuPc thin film may be doped. When the surface is modified by an octadecylphosphonic acid (ODPA) monolayer, the DOS increases, and the peak near E = 0 eV becomes sharper.

Unlike the reported exponential decrease of the DOS on CuPc/OTS/SiO_2,[28] we find that the DOS of CuPc on ATO and ODPA-modified ATO can be divided into a core level of the HOMO, which can be fitted with a Gaussian distribution, and a tail that is extended into the gap. To estimate the bandwidth of the HOMO, the Gaussian distribution[18] in the following expression is used:

$$g(E) = \left[\frac{N_0}{\sigma\sqrt{2\pi}}\right] \exp\left[-\left(\frac{E - E_c}{\sqrt{2}\,\sigma}\right)^2\right] \tag{2}$$

where N_0 is the total density of states of the HOMO, E_c is the center of the HOMO, and σ is the Gaussian width. We fit the DOS using a total state density of 1.70×10^{21} cm^{-3} for α-phase CuPc, which corresponds to the condition that one molecule contributes one state.

For the CuPc/ATO, we observe a HOMO Gaussian width of 0.33 ± 0.02 eV and centers at −1.06 ± 0.04 eV. On the ATO substrate, a pinning effect is not observed. The minimum concentration of the trap states measured in the band gap is about 7×10^{17} cm^{-3}. This value is lower than most of the OFETs (>10^{18} cm^{-3}) and approaches those of the single-crystal OFETs (10^{15}−10^{19} cm^{-3}).[30] Two aspects are responsible for the reduction in the trap states. The first one is the better crystallinity of CuPc on ATO. Figure 4 shows the surface morphologies of CuPc on SiO_2 and ATO with a nominal thickness of 5 nm. The CuPc molecules on SiO_2 form a rodlike structure and are intertwined with each other in different layers. Although the CuPc thin film grown on ATO also shows similar rodlike shape, they interconnect with each other, forming a continuous smooth interfacial network. The interlayer thickness obtained from the top layer is around 1.3−1.4 nm, corresponding to the a axis of the α-phase CuPc.[31] The α-phase structure of CuPc is also confirmed by X-ray diffraction (XRD; Figure S3a in the Supporting Information). Traps are always generated at the boundaries; therefore, the smaller size of the crystal domain is expected to have larger density of traps. The crystal domain size can be estimated from the AFM images (Figure S3b in the Supporting Information). The width and length of the CuPc rods on ATO are slightly larger than the respective parameters of CuPc on SiO_2. Besides the domain size, the in-plane ordering in the molecular layer is another major concern. A discernible diffraction peak of (1, 0) is observed on a 2.4-nm-thick CuPc film on ATO from the GIXD pattern (inset in Figure 4b). In contrast, no peak is observed from CuPc on SiO_2 (inset in Figure 4a). The above results indicate that CuPc grown on ATO possesses better in-plane ordering than that on SiO_2. The improved short-range ordering in the CuPc domain on ATO results in fewer intrinsic traps, which greatly enhances the mobility.

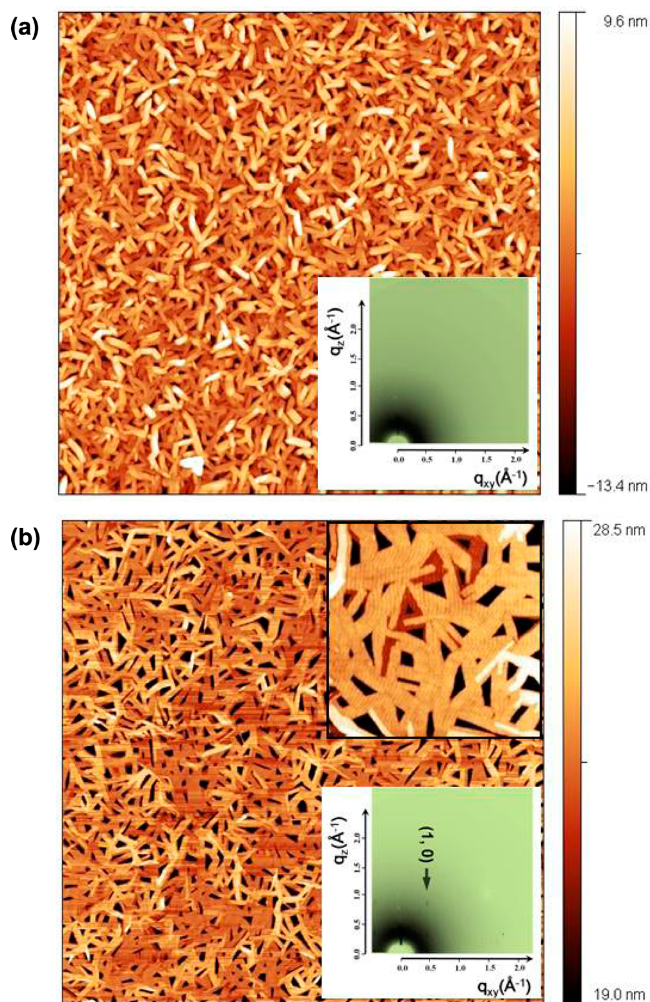


Figure 4. AFM morphology of 5-nm-thick CuPc on SiO_2 (a) and ATO (b) substrates (5×5 μm^2). The insets in the lower-right of parts a and b show the GIXD images of a CuPc thin film with a thickness of 2.4 nm on the substrates. The inset in the upper-right in part b is the zoom in image of 1×1 μm^2.

The second reason can be attributed to the optimized interface properties. The measured contact angle of deionized water on the ATO substrate is 35.5°, which is larger than that on the SiO_2 substrate (<5°). The observation indicates a

reduction in the surface energy on the ATO substrate, which makes the surface more unfavorable for water absorption in air and leads to a reduction of the concentration of the hydroxyl group. The hydroxyl groups ($-OH^-$) at the surface are regarded as highly polarized species, which induce interfacial dipoles at the interface. The existence of interface dipole is confirmed by the thickness-dependent vacuum level in the $CuPc/SiO_2$ system, as shown in Figure 5. The $-OH^-$ group at the surface of SiO_2 attracts holes in CuPc and thus results in an upward vacuum level bending from −274.0 to −193.6 meV with decreasing CuPc thickness from 25 to 5 nm. On the other hand, it is found that the vacuum level of CuPc remains at around −300 meV on the ATO substrate, suggesting a lower density of interface dipoles.

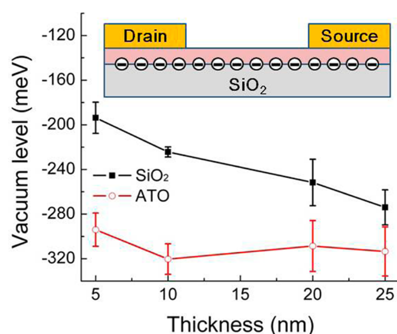
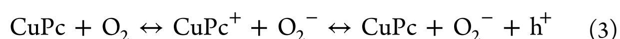


Figure 5. Thickness-dependent band bending of the CuPc thin film on SiO_2 and ATO substrates.

Besides the above two aspects, chemical impurities in organic semiconductors can also introduce traps; for example, oxidized species in a pentacene single crystal are believed to act as scattering centers.[32] In the DOS of CuPc on ATO, a small peak near the HOMO edge can be observed, and the Gaussian fitting using eq 2 shows that the DOS centers at 0.165 eV. This peak becomes obvious after ODPA modification. A previous report on the DOS of a rubrene single crystal shows that oxygen exposure induces a strong peak at the HOMO edge.[16] Photoemission yield spectroscopy measurement on the CuPc thin film after oxygen exposure reveals that the Fermi level shifts to the HOMO compared with the freshly deposited CuPc surface,[33] indicating the existence of oxygen-induced gap states between the Fermi level and the HOMO band. It is reported that O_2 adsorption improved the electrical properties of CuPc,[34,35] which suggests that O_2 is a hole dopant. To confirm this idea, we remove the oxygen effect by evacuating the chamber to a vacuum of 10^{-5} Pa. We find that the mobility of the CuPc/ATO device decreases greatly (Figure 3b). This finding confirms that the adsorbed oxygen species in the CuPc film does not trap carriers but acts as a dopant to improve the p-type performance of the device. Therefore, the peaks at the HOMO edge are assigned to the doping level induced by the absorbed oxygen. The doping of O_2 can be described by



$$\mathrm{CuPc} + \mathrm{O_2} \leftrightarrow \mathrm{CuPc}^+ + \mathrm{O_2}^- \leftrightarrow \mathrm{CuPc} + \mathrm{O_2}^- + \mathrm{h}^+ \quad (3)$$

The holes in the oxygen-induced doping level near the HOMO edge are thermally exited to the HOMO of CuPc, and it also enables the shallow trap states to be filled at the interface.[36] The peak doping DOS in the case of the ODPA surface is only 5.3×10^{19} cm^{-3}, which is smaller than the trap concentration on the SiO_2 surface, so the doping effect is not observed at the interface of $CuPc/SiO_2$.

It has been suggested that an increase of the k value will lead to interfacial dipolar disorder, which decreases the device mobility.[11] At the CuPc/ATO interface, a wide distribution of DOS is observed. Surface modification is an effective way to reduce the dipolar disorder effect.[37] To decrease the dipolar effect, we modified the surface of ATO using an ODPA monolayer, and a reduced DOS width of 0.08 ± 0.01 eV is observed (Figure 3a). Because ODPA modification does not obviously affect the surface morphology of CuPc, the narrow DOS distribution after ODPA modification should result from the reduction of dipolar disorders. However, no improvement in the mobility of the CuPc device is observed by ODPA modification (Figure S4 in the Supporting Information), indicating that the dipolar disorder is not a dominating limitation of carrier mobility when ATO is used as the gate dielectric. On the other hand, because ambient doping increases the mobility of the device, we therefore infer that the extra carriers generated by the doping level contribute to the enhanced mobility. The dipolar disorder effect can render localization of charge carriers near the HOMO edge, and at the same time, the doping level is also located at the HOMO edge. As a result, we deduce that the carrier doping should compensate for the band-edge localization effect so that the dipolar disorder effect is not obvious in the CuPc/ATO device.

The carrier density can be estimated from $C_{ox}(V_{GS} - V_T)/e$. The interfacial carrier density is 2.34×10^{12} cm^{-2} for the CuPc/ATO device at a gate bias of −3 V and 4.11×10^{12} cm^{-2} for the $CuPc/SiO_2$ device at a gate bias of −60 V. This reveals a lower density of the interfacial carrier in the CuPc/ATO device than in the $CuPc/SiO_2$ device. However, the trap density is also much lower in the former device. Furthermore, the doping effect of ambient conditions also brings about a reduction of the disorder effect. Therefore, the superior performance of the CuPc/ATO device should be attributed to a combination of the low-trap DOS in the gap and doping effects.

In addition to the channel effect, we note that the contact effect is also affected by the interfacial dipoles. The contact effect can be evaluated from the potential distribution along the channel of devices, as shown in Figure 2a,b. It is observed that the minimum contact resistances of the source and drain electrodes in the CuPc/ATO device are similar at $V_{DS} = -0.8$ V, and the contact resistance takes up 27.6% of the total resistance. By contrast, the minimum drain contact resistance of the $CuPc/SiO_2$ device is about 7 times larger than that of the source electrode, and they take up 36% of the total resistance. The difference of the contact resistance of source and drain electrodes can be partially understood by the interfacial dipoles, as shown in the inset of Figure 5. The $-OH^-$ groups induce interfacial dipoles at the electrodes, which induce an electrical field along the same direction as the gate field. The combined electric field improves hole injection from the source electrode to the channel. At the drain side, on the other hand, the electrical field of the dipoles is in the opposite direction of the applied electrical field, and hence holes injected from the CuPc channel into the drain electrode have to overcome the dipoles underneath. Therefore, the contact resistance of the drain electrode is higher than that of the source electrode. In the case of CuPc/ATO, the interfacial dipole is weak, so the source and drain electrodes are similar by and large.

■ SUMMARY

We have measured the interfacial transport properties and DOS of CuPc on SiO_2, ATO, and ODPA/ATO gate dielectrics using

the KPFM method under air conditions. The HOMO edge of CuPc on SiO_2 is pinned under ambient conditions. CuPc on a high-*k* ATO substrate shows a Gaussian width of 0.33 ± 0.02 eV. A low-trap DOS of 7×10^{17} cm^{-3} in the gap is observed in CuPc on the ATO substrate. The low-trap DOS is due to the improved crystallinity of CuPc and reduced surface dipoles. In addition, an obvious energy level is observed at the HOMO edge, which is assigned to the oxygen doping level. ODPA modification on ATO is used to reduce the high-*k* dielectric dipolar effect. A sharpened DOS is observed after modification. However, the modified device does not show improved mobility. We postulate that the dipolar disorder effect is probably compensated for by the oxygen doping effect. The superior performance of the CuPc/ATO device is attributed to the low-trap DOS and doping effect. The findings enrich the understanding the interfacial DOS of organic TFTs and will help to reveal the transport mechanism of organic semiconductors.

ASSOCIATED CONTENT

Supporting Information

Experimental details to prepare the dielectric, KPFM characterization detail, XRD patterns of CuPc, and device performance of CuPc/ODPA/ATO. This material is available free of charge via the Internet at http://pubs.acs.org.

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Notes

The authors declare no competing financial interest.

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